



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/713,733	11/13/2003	Elmootazbellah Nabil Elnozahy	AUS920030760US1	2697
45992	7590	10/20/2006	EXAMINER	
IBM CORPORATION (JVM) C/O LAW OFFICE OF JACK V. MUSGROVE 2911 BRIONS WOOD LANE CEDAR PARK, TX 78613			SAVLA, ARPAN P	
			ART UNIT	PAPER NUMBER
			2185	

DATE MAILED: 10/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/713,733	Applicant(s) ELNOZAHY ET AL.	
	Examiner Arpan P. Savla	Art Unit 2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 14 July 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-23 is/are pending in the application.
- 4a) Of the above claim(s) 21-23 is/are withdrawn from consideration.
- 5) ☒ Claim(s) 1-6 is/are allowed.
- 6) ☒ Claim(s) 7-20 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Amendment

This Office action is in response to Applicant's communication filed July 14, 2006 in response to the Office action dated April 14, 2006. Claim 13 has been amended. Claims 21-23 remain withdrawn. Claims 1-23 are pending in this application.

REJECTIONS NOT BASED ON PRIOR ART

Claim Rejections - 35 USC § 112

1. In view of Applicant's amendment, the 112 rejection to claim 13 has been withdrawn.

REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 7, 9-17, and 19-20 are rejected under U.S.C. 102(b) as being anticipated by Armangau (U.S. Patent 6,434,681).
4. As per claim 7, Armangau discloses a memory controller comprising:

an input for receiving page remapping instructions (col. 6, lines 42-48; Fig. 1, elements 20, 21, and 24); *It should be noted that the "back command" is analogous to "remapping instructions."*

a mapping table which temporarily stores entries of old page addresses and corresponding new page addresses associated with the page remapping instructions (col. 7, lines 18-20; Fig. 1, element 26). *It should be noted that the "primary directory" is analogous to the "mapping table."*

and a memory access device which directs the copying of memory pages from the old page addresses to the new page addresses and releases the entries in said mapping table as copying for each entry is completed (col. 6, lines 42-50; col. 7, line 65 – col. 8, line 3; Fig. 1, element 21). *It should be noted that the "primary data storage subsystem" provides the functionality of a "memory access device."*

5. **As per claim 9**, Armangau discloses said memory access device directs a read operation for a new page address which is currently being copied to a corresponding old page address (col. 2, lines 16-18).

6. **As per claim 10**, Armangau discloses said memory access device directs a write operation for a new page address which is currently being copied to both the new page address and a corresponding old page address (col. 15, line 52 – col. 16, line 13; Fig. 7B, elements 124-129).

7. **As per claim 11**, Armangau discloses said memory access device directs a write operation for a new page address which has not yet been copied to a corresponding old page address (col. 15, lines 43-51; Fig. 7B, elements 122 and 123).

8. **As per claim 12**, Armangau discloses said memory access device includes a state engine which sequentially reads the paired old and new pages addresses in said mapping table (col. 6, lines 42-48; Fig. 1, element 21). *It should be noted that the "primary data storage subsystem" provides the functionality of a "state engine."*

9. **As per claim 13**, Armangau discloses said memory access device further includes a direct memory access (DMA) engine controlled by said state engine which carries out actual copying of the memory pages (col. 8, lines 4-9; col. 13, lines 17-28; Fig. 1, element 65). *It should be noted that the "snapshot copy facility" is analogous to the "DMA engine."*

10. **As per claim 14**, Armangau discloses a computer system comprising:
a processing unit (col. 6, lines 1-2; Fig. 1, element 20);
an interconnect bus connected to said processing unit (Fig. 1, the "line" (i.e. bus) between the host the primary data storage subsystem)
a memory array (col. 6, lines 3-6; Fig. 1, element 27);
and a memory controller connected to said interconnect bus and said memory array, wherein said memory controller copies memory pages from old page addresses to new page addresses while said processing unit carries out program instructions using the new page addresses (col. 6, lines 42-50; Fig. 1, element 21). *It should be noted that the "primary storage subsystem" provides the functionality of a "memory controller."*

11. **As per claim 15**, Armangau discloses said processing unit includes a processor core having a translation lookaside buffer (TLB) whose entries keep track of current

virtual-to-physical memory address assignments (col. 7, lines 18-20; Fig. 1, element 26); *It should be noted that the "primary directory" is analogous the "TLB."*

and said TLB entries are updated for the new page addresses prior to completion of copying of the memory pages by the memory controller (col. 7, lines 49-64).

12. **As per claim 16**, Armangau discloses said processing unit has a processor core and an associated cache (Fig. 1, element 21; Fig. 3, element 52);

and said cache modifies an address tag of a cache entry which corresponds to a memory location in the new page addresses (col. 10, lines 50-54). *It should be noted that the primary directory within the cache contains addresses to memory locations in the new versions of the physical units.*

13. **As per claim 17**, Armangau discloses said cache modifies the address tag of the cache entry in response to a determination that the cache entry contains a valid value which is not present elsewhere in the system (col. 10, lines 50-67).

14. **As per claim 19**, Armangau discloses said memory controller includes:

a mapping table which temporarily stores entries of old page addresses and corresponding new page addresses (col. 7, lines 18-20; Fig. 1, element 26); *See the citation note for the similar limitation in claim 7 above.*

and a memory access device which directs the copying of the memory pages from the old page addresses to the new page addresses and releases the entries in said mapping table as copying for each entry is completed (col. 6, lines 42-50; col. 7, line 65 – col. 8, line 3; Fig. 1, element 21). *See the citation note for the similar limitation in claim 7 above.*

15. **As per claim 20**, Armangau discloses said processing unit, said interconnect bus, said memory array and said memory controller are all part of a first processing cluster, and further comprising a network interface which allows said first processing cluster to communicate with a second processing cluster, said memory controller having at least one pointer for a new page address which maps to a physical memory location in said second processing cluster (col. 6, lines 1-3; Fig. 1, element 22). *It should be noted that the "second storage subsystem" is analogous to the "second processing cluster." It should also be noted that it is inherently required the second storage subsystem include some sort of "interface" in order to communicate with the first storage subsystem.*

Claim Rejections - 35 USC § 103

16. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

17. **Claim 8 is rejected under 35 U.S.C. 103(a) as being obvious over Armangau in view of Romer et al. "Reducing TLB and Memory Overhead Using Online Superpage Promotion", hereafter "Romer."**

18. Armangau discloses all the limitations of claim 8 except said mapping table has 32 slots for receiving corresponding pairs of the old page addresses and new page addresses.

Romer discloses said mapping table has 32 slots for receiving corresponding pairs of the old page addresses and new page addresses (pg. 178, italicized section entitled "Table 2", line 4). *It should be noted that the "entries" is analogous to the "slots."*

Armangau and Romer are analogous art because they are from the same field of endeavor, that being computer memory mapping systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Armangau's primary directory as Romer's 32 TLB.

The motivation for doing so would have been to improve system performance by increasing instructions per TLB miss (Romer, pg. 187, section entitled "Capacity Counters", last paragraph).

Therefore, it would have been obvious to combine Armangau and Romer for the benefit of obtaining the invention as specified in claim 8.

19. Claim 18 is rejected under 35 U.S.C. 103(a) as being obvious over Armangau in further view of Evans et al. (U.S. Patent 6,732,238).

20. Armangau discloses all the limitations of claim 18 except said cache further relocates the cache entry based on a changed congruence class for the modified address tag.

Evans discloses said cache further relocates the cache entry based on a changed congruence class for the modified address tag (col. 4, lines 27-34; col. 7, lines 48-64). *It should be noted that "associativities with different number of indices" is analogous to "different congruence classes."*

Armangau and Evans are analogous art because they are from the same field of endeavor, that being computer memory systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Evans's TLB replacement algorithm within Armangau's primary directory.

The motivation for doing so would have been an efficient and scalable implementation that provides good performance on the level of LRU, random, and clocked replacement algorithms (Evans, col. 4, lines 35-37).

Therefore, it would have been obvious to combine Armangau and Evans for the benefit of obtaining the invention as specified in claim 18.

Response to Arguments

21. Applicant's arguments, filed July 14, 2006, with respect to the rejections of claims 1-20 under 103(a) using the Arimilli reference (U.S. Patent 6,907,494) have been fully considered and are persuasive in view of the "Declaration To Disqualify Prior Art Under U.S.C. §103(c)" filed July 14, 2006. Therefore, the rejections have been withdrawn. However, upon further consideration, new grounds of rejection have been made under 35 USC 102(b) with respect to claims 7, 9-17, and 19-20 and 35 USC 103(a) with respect to claims 8 and 18 as presented above.

STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the application as recommended by MPEP 707.70(i):

Allowable Subject Matter

22. **Claims 1-6** are allowed.

23. The following is an examiner's statement of reasons for allowance:

The prior art of record fails to disclose the combination including the limitations of:

(Claim 1) "...accessing at least one of the virtual memory pages using the new virtual superpage mapping while the memory controller is copying old physical memory pages to new physical memory pages."

24. As dependent **claims 2-6** depend from an allowable base claim, they are at least allowable for the same reasons as noted above.

Claims Rejected in the Application

25. Per the instant office action, **claims 7-20** have received a second action on the merits and are subject of a second action non-final.

RELEVANT ART CITED BY THE EXAMINER

The following prior art made of record and not relied upon is cited to establish the level of skill in Applicant's art and those arts considered reasonably pertinent to Applicant's disclosure. See MPEP 707.05(e).

Art Unit: 2185

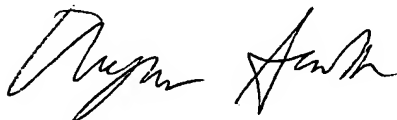
1. U.S. Patent 5,206,939 (Yanai et al.) discloses a system and method for disk mapping and data retrieval
2. U.S. Patent 6,477,612 (Wang) discloses providing access to physical memory allocated to a process by selectively mapping pages of the physical memory with virtual memory allocated to the process.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Arpan P. Savla whose telephone number is (571) 272-1077. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah can be reached on (571) 272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2185

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



Arpan Savla
Art Unit 2185
October 15, 2006


10/16/06

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER